In the claims

1. (original) A hardware counter comprising:

a memory array storing a plurality of counter values indexable by an index constructed based at least on a number of a plurality of events to which the counter values correspond; and,

a hardware incrementer to read the counter values from the memory array by values of the index, increment the counter values, and write the counter values as incremented back into the memory array.

2. (original) The hardware counter of claim 1, wherein the index is constructed as a number of bits binarily representing the number of the plurality of events.

3. (original) The hardware counter of claim 1, wherein the index is constructed further based on a number of a plurality of qualifiers to the plurality of events.

4. (original) The hardware counter of claim 3, wherein the index is constructed as a concatenation of a number of bits binarily representing the number of the plurality of events and a number of bits binarily representing the number of the plurality of qualifiers, such that each counter value corresponds to a unique combination of one of the plurality of events and one of the plurality of qualifiers.

5. (original) The hardware counter of claim 3, wherein the index is constructed as a number of bits binarily representing a number of possibly occurring event-and-qualifier combinations, such that each counter value corresponds to a different one of the possibly occurring event-and-qualifier combinations, wherein a number of counter values is less than the number of the plurality of events multiplied by the number of the plurality of qualifiers.

6. (original) The hardware counter of claim 5, further comprising index generation hardware to generate a value of the index for an input one of the possibly occurring event-and-qualifier combinations.

7. (original) The hardware counter of claim 1, wherein the hardware incrementer comprises a hardware adder that adds an increment value to the counter values, such that results of adding the increment value to the counter values is written back into the memory array.

8. (original) The hardware counter of claim 7, wherein the hardware incrementer further comprises a register storing the increment value.

9. (original) The hardware counter of claim 1, further comprising:

index generation hardware to generate the index; and,

hardware to read the counter values from the memory array by the values of the index and write the counter values to the memory array.

10. (original) The hardware counter of claim 1, wherein the memory array is divided into a plurality of memory banks over which the plurality of counter values are stored, each memory bank having a separate instance of the hardware incrementer.

11. (original) The hardware counter of claim 10, wherein the index globally indexes the plurality of counter values over the plurality of memory banks as a whole.

12. (original) The hardware counter of claim 10, wherein each memory bank has a separate instance of the index that indexes only those of the plurality of counters stored in the memory

bank, each memory bank having associated therewith index generation hardware to generate the separate instance of the index for the memory bank.

13. (original) A method comprising:

generating via hardware a value of an index based on one of a plurality of events, a count value for an occurrence of which is to be incremented;

reading by the value of the index the counter value from a memory array indexed by the index;

incrementing via hardware the counter value; and,

writing the counter value as incremented back into the memory array.

14. (original) The method of claim 13, wherein generating via hardware the value of the index comprises generating via hardware the value of the index based on the one of the plurality of events and one of a plurality of qualifiers to the events.

15. (original) The method of claim 14, wherein generating via hardware the value of the index comprises generating the index as one of:

a concatenation of a number of bits binarily representing the number of the plurality of events and a number of bits binarily representing the number of the plurality of qualifiers; and,

a number of bits binarily representing a number of possibly occurring event-and-qualifier combinations, such that each counter value corresponds to a different one of the possibly occurring event-and-qualifier combinations.

16. (original) A system comprising a plurality of nodes, each node having a processor and a performance counter operatively coupled to the processor to count occurrences of events, the

performance counter having a lesser number of hardware incrementers than a number of the events of which the performance counter counts the occurrences.

17. (original) The system of claim 16, wherein the performance counter counts occurrences of combinations of events and qualifiers, the performance counter having a lesser number of the hardware incrementers than a number of the combinations of the events and the qualifiers of which the performance counter counts the occurrences.

18. (original) The system of claim 16, wherein the performance counter comprises a memory array storing counter values for counting the occurrences of the events, and a single hardware incrementer to increment the counter values of the memory array in response to the occurrences of the events to which the counter values correspond.

19. (original) The system of claim 16, wherein the performance counter comprises a plurality of memory banks and a plurality of hardware incrementers corresponding to the memory banks, each memory bank storing counter values for counting the occurrences of some of the events, each hardware incrementer incrementing the counter values of the memory bank to which the hardware incrementer corresponds in response to the occurrences of the some of the events to which the counter values of the hardware incrementer correspond.

20. (original) The system of claim 16, wherein each node further comprises memory that is local to the processor of the node and remote to the processor of every other of the nodes.